Office Action Summary	Application No.	Applicant(s)	
	09/190,378	ALBERT, DOUGLAS M.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☐ Responsive to communication(s) filed on *03 April 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1- 32* is/are pending in the application.

4a) Of the above claim(s) *25-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) *28-32* is/are objected to.

8)☐ Claims *1-27* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Applicants' amendment filed April 03, 2000 has been entered. Therefore claim 1 as amended by the amendment , claims 2-27 as originally filed are pending in the application. New Claims 28-32 attempted to be added by the amendment have been rejected for the reasons stated below.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121: I. Claims 1-24, are drawn to a method of manufacturing thinned integrated circuits classified in class 438, subclass 460.

II. Claims 25-27, are drawn to an assembly (device) , classified in class 257, subclass 458

Inventions Groups I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the recited devices (assembly) product as claimed can be made by another and materially different process namely first securing the wafer to the rigid substrate and then forming grooves from the back side and separating the wafers.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

During a telephone conversation with Joseph C. Andras Esq. on Sept. 23, 2000 @ (714) 444-1199 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-24. Affirmation of this election must be made by applicant in replying to this Office action. Claims 25-27 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Request to Institute Interference - Denied

Applicants in their preliminary amendment had request that an interference be set up with issued patent to Sasaki et al. (U.S. Patent No. 5,888,883, herein after Sasaki) however the request is denied because the Applicants' have attempted to show support for their alleged counts on their CIP application filed Nov. 10, 1998 and not on the Parent provisional Application No. 60/ 065088 filed Nov. 11, 1997. Therefore the only logical conclusion is that their provisional application identified above (60/060588) does not have the disclosure to support the counts.

The Sasaki U.S. patent claims a priority from Japanese Application No. 9-197291 filed July 23, 1997. Therefore Sasaki as a WTO country filed application

can claim his invention at least as far back as July 23, 1997 much before the Nov. 10, 1998 date of the instant U.S. Application.

Further more even the specification filed Nov. 10, 1998 lacks disclosure of the elements/ steps as shown below.

Therefore the Applicants' have failed to show that they had invented the elements/steps of their proposed count at least till Nov. 10, 1998 therefore the request for the interference is denied.

Claim Rejections - 35 USC § 112

Claims 28-32 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicants' have attempted to find support in the specification as filed Nov. 11, 1998 however the support is totally lacking atleast for the following exemplary elements in the specification filed on November 11, 1998.

1) the grooves being deeper than a finished thickness of the chip. If applicants' contention is correct than how is the chip still attached to the wafer after the formation of the grooves ?

2) Lapping . the lapping step is not mentioned or described in the specification filed November 11, 1998.

3) the depth of the groove is greater than the thcikness of the finished chip by atleast 5 nm. See 1) above.

Therefore independent claims 28 and 31 and dependent claims 29-30 and 32 are all rejected under 35 U. S.C. Section 112.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 –24 are rejected under 35 U.S.C. 102(b) as being anticiapted by Sasaki et al. (U. S. Patent No. 5,888,883, herein after Sasaki).

As shown above Applicants' did not invent their invention at the earliest as of Nov. 10, 1998.

With respect to claim 1, Sasaki teaches a method of manufacturing a plurality of thinned integrated circuits from a wafer having front and backside surfaces and a thickness including the steps of : defining a plurality of grooves in the front surface (Sasaki fig. 8 # 22, col. 6 line 49-50), the grooves being of a depth less than the thickness of the wafer so that the plurality of dies remain attached to the wafer. Mounting the wafer on a flat rigid surface with the front side of the wafer turned towards the rigid surface (Sasaki figs. 10 & 11 # 26, col. 6 line 60-col. 7 line 36), mechanically removing a predetermined portion of back side of the wafer until the thickness of the wafer is reduced to expose the dies . (Sasaki fig. 11 , col. 7 lines 21-24), releasing the plurality of dies from the substrate (Sasaki fig. 12 , col. 7 lines 39-50).

With respect to claim 2, Sasaki teaches a method of manufacturing a plurality of thinned integrated circuits from a wafer having front and backside surfaces and a thickness including the steps of : forming a planarizing layer of low stress material on the front surface of the wafer (Sasaki, fig. 10 # 21, Col. 6 lines 60-67).

With respect to claims 3 and 7 , Sasaki teaches a method of manufacturing a plurality of thinned integrated circuits from a wafer having front and backside surfaces and a thickness including the steps of : forming a layer of low stress material o the front surface of the wafer (Fig. 8 # 21, col. 6 lines 33-53). The grooves being 50 microns deep (Col.8 line 49-50).

With respect to claims 4 and 5, Sasaki teaches a method of manufacturing a plurality of thinned integrated circuits from a wafer having front and backside surfaces and a thickness including the steps of : affixing an optically flat surface to the wafer front surface (See teachings under 2 and 3 above).

With respect to claims 6 , 10,11, 18 and 19 Sasaki teaches a method of manufacturing a plurality of thinned integrated circuits from a wafer having front and backside surfaces and a thickness including the steps of :

Disposing a polyimide layer on the wafer front surface (Saski col. 8 lines 10-76) .

With respect to claims 8 and 9, Sasaki teaches a method of manufacturing a plurality of thinned integrated circuits from a wafer having front and backside surfaces and a thickness including the steps of :

Wherein wafer thickness after removal is 25-50 microns or less (Sasaki col.51-52).

With respect to claim 12, Sasaki teaches a method of manufacturing a plurality of thinned integrated circuits from a wafer having front and backside surfaces and a thickness including the steps of :

Wherein the dies are released by placing them on a pin block and dissolving the adhesive (Sasaki Fig. 12 , col. 7 line 39-45).

With respect to claims 13 and 14 , Sasaki teaches a method of manufacturing a plurality of thinned integrated circuits from a wafer having front and backside surfaces and a thickness including the steps of : mounting dies on a flexible film (Sasaki fig. 13 # 35, col. 7 lines 46-53).

With respect to claims 13 and 14 , Sasaki teaches a method of manufacturing a plurality of thinned integrated circuits from a wafer having front and backside surfaces and a thickness including the steps of : electrically coupling the ic with metalizations coupled with epoxy (Sasaki col. 7 line 51-55).

With respect to claim 17 , Sasaki teaches a method of manufacturing a plurality of thinned integrated circuits from a wafer having front and backside surfaces and a thickness including the steps of : wherein the plurality of grooves facilitate the flow of material (Sasaki figs. 9 and 12 , col. 2 line 33-37).

With respect to claims 20, 21 and 22, Sasaki teaches a method of manufacturing a plurality of thinned integrated circuits from a wafer having front and backside surfaces and a thickness including the steps of :

Wherein the grinding step includes a dwell and non dwell cycles, advance reduction rates (inherent in grinding, also see Sasaki fig. 8 and dry chemical etch or mechanical polish (Il well known processes , also see Sasaki col.7 lines 1-15).

With respect to claims 23 and 24, Sasaki teaches a method of manufacturing a plurality of thinned integrated circuits from a wafer having front and backside surfaces and a thickness including the steps of:

Wherein the grooves are linear in and in a grid fashion (Sasaki figs. 5,6, 8 and 11, col. 2 lines 12-17 , etc.) and the wherein the separated dies are stacked and electrically inter connected . (Sasaki figs. 12 and 13, col.7 lines 47-50).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is 703-306-5945. The examiner can normally be reached on M-F, 8.00 to 5.00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703- 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703- 308-0956.

SR

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September 28, 2000